Customizable ASIC Test Stand

Customizable ASIC Test Stand Features

1. Provides a quick and easy means of testing new ASICs

2. Leverages highly documented, platform independent, zero cost, open source TCL-based software

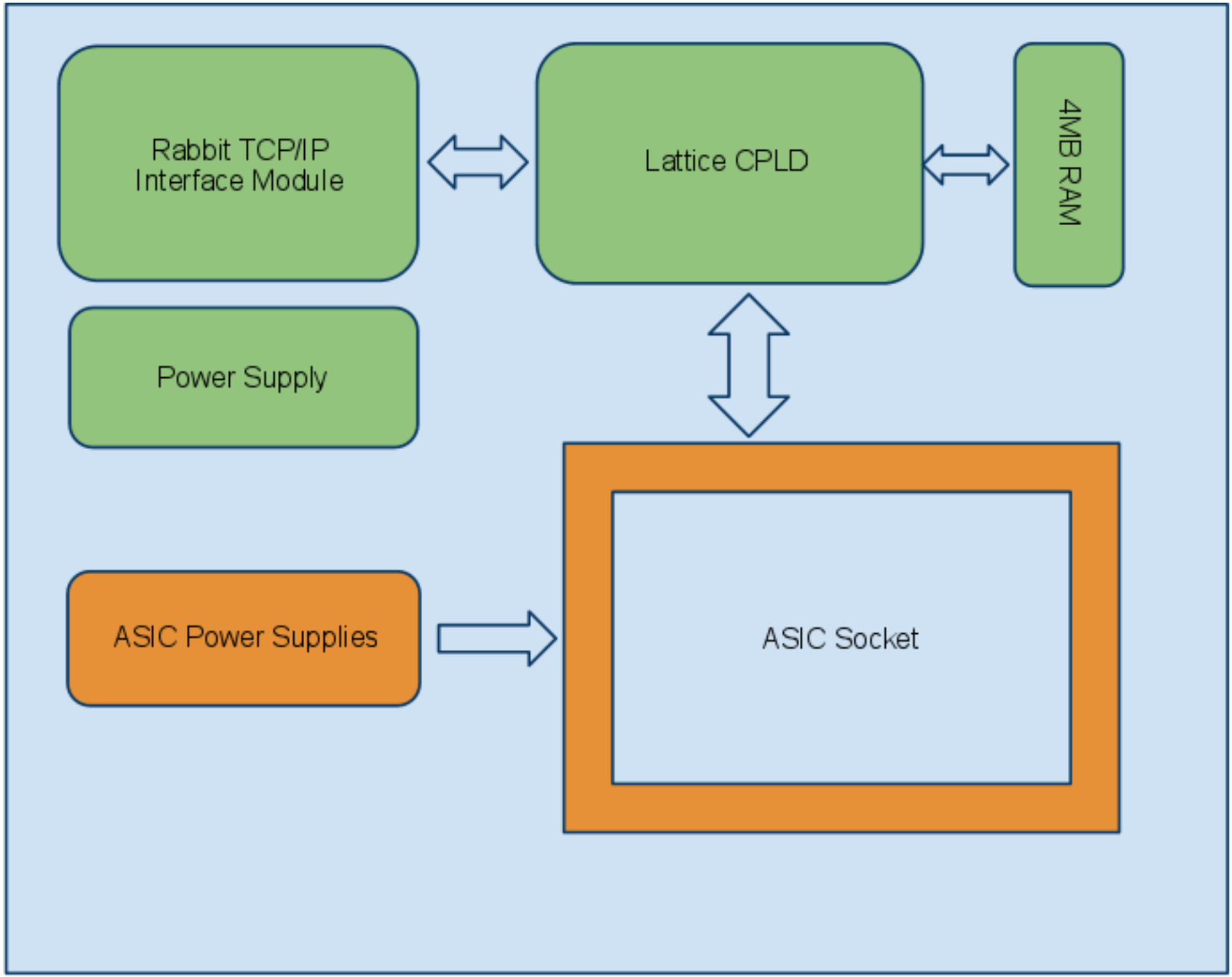
3. Utilizes a 50% complete pcb layout.

4. Come with a set of over 50 standard, reliable commands meant to send and receive data between the host computer and the CPLD.

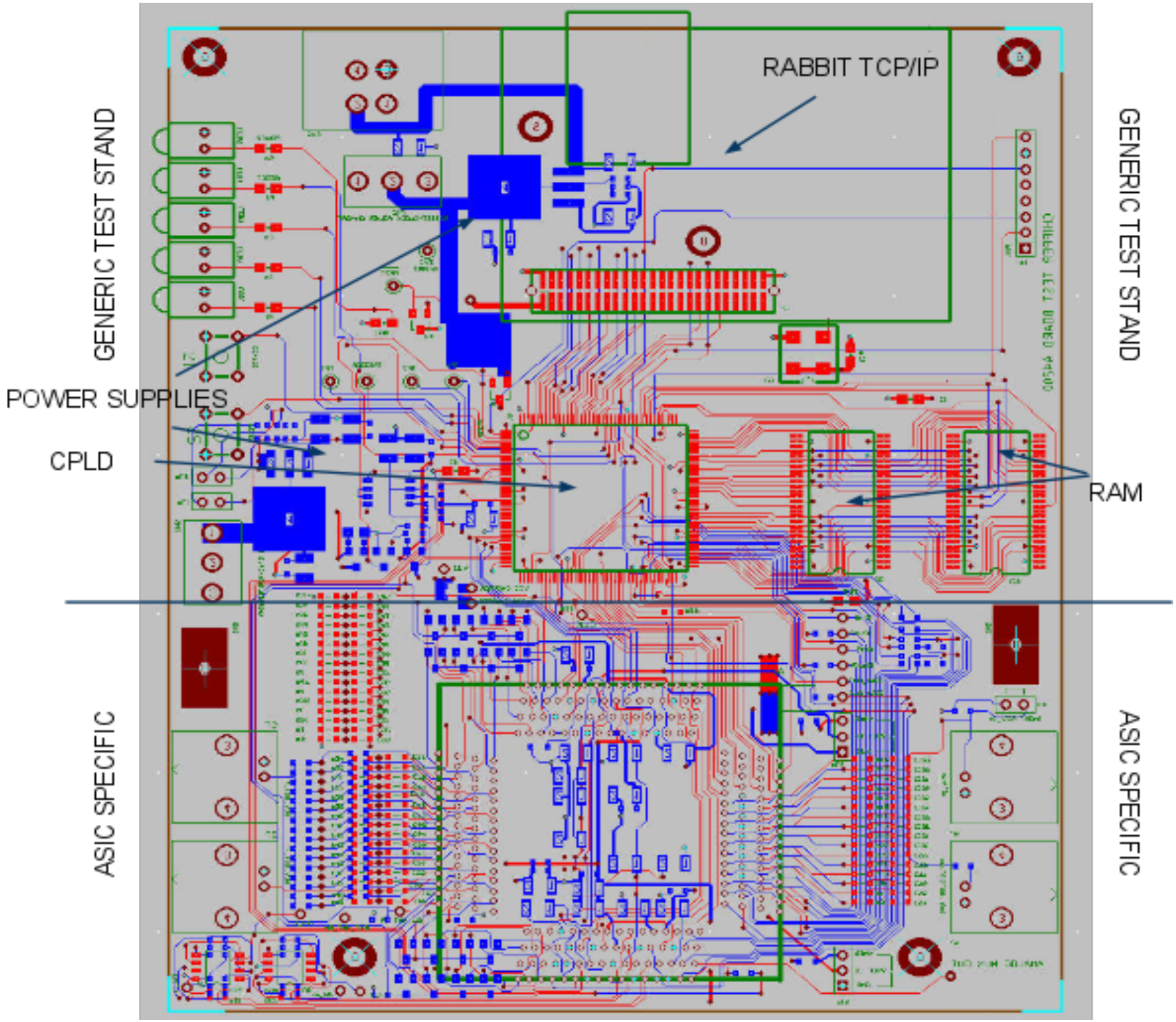
5. Because the interface from computer to CPLD is the same for each customized test stand, the user can write and verify new test software/firmware before the layout is complete. In fact, the user can use any previously laid out test stand.

6. TCP/IP based communication.

Generic Test Stand Diagram



Chipper Test Board Layout



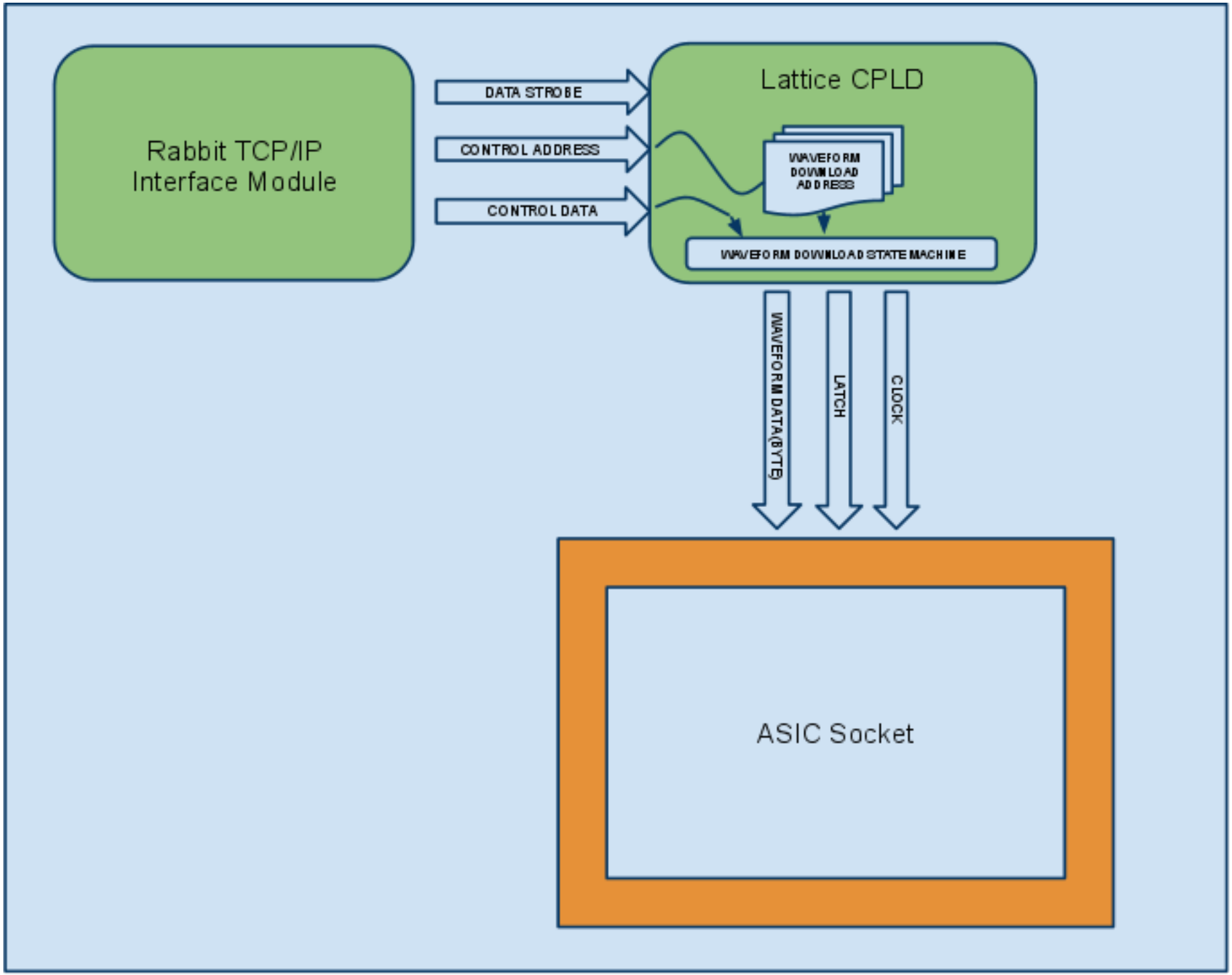
How to adapt the Generic Test Stand for a new ASIC

1. The generic test stand layout comes with the CPLD-RAM-TCP/IP electronics pre-laid out. The user only needs to layout out electronics specific to the ASIC such as the socket, power supplies, input/output connectors, and connections between the CPLD and ASIC (serial/parallel download lines, scan chain outputs,etc).

2. Modify CPLD firmware to account for newly defined pin connections between CPLD and ASIC. Also add firmware to account for functions specific to ASIC interactions.

3. Add/modify TCL script to account for newly defined functions specific to ASIC interactions. Writing new scripts requires only a simple text editor. No compilation necessary.

Waveform Download Diagram



Example Firmware and TCL script to add a new function

Step ONE - Create a TCL/Tk Button:

```
button $c.downwaveform -text "Download_Waveform" -command download_waveform
pack $c.downwaveform
```

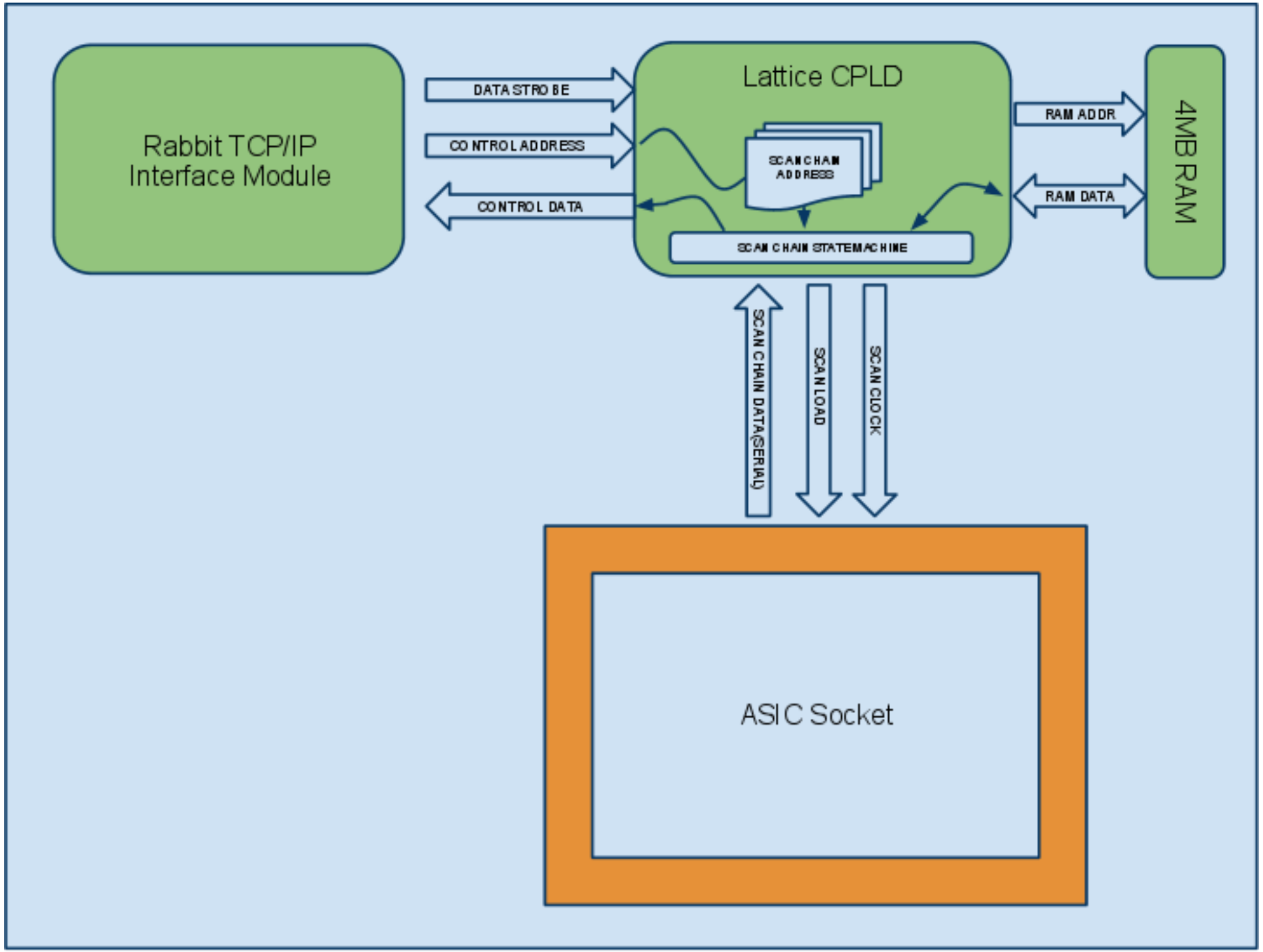
Step TWO - Create a TCL/Tk procedure:

```
proc download_waveform {} {
        set sock [LWDAQ_socket_open 10.0.0.37:90]
                set data [binary format c* $sinewave]
    LWDAQ_stream_write $sock 8 $data
   LWDAQ_socket_close $sock
}
```

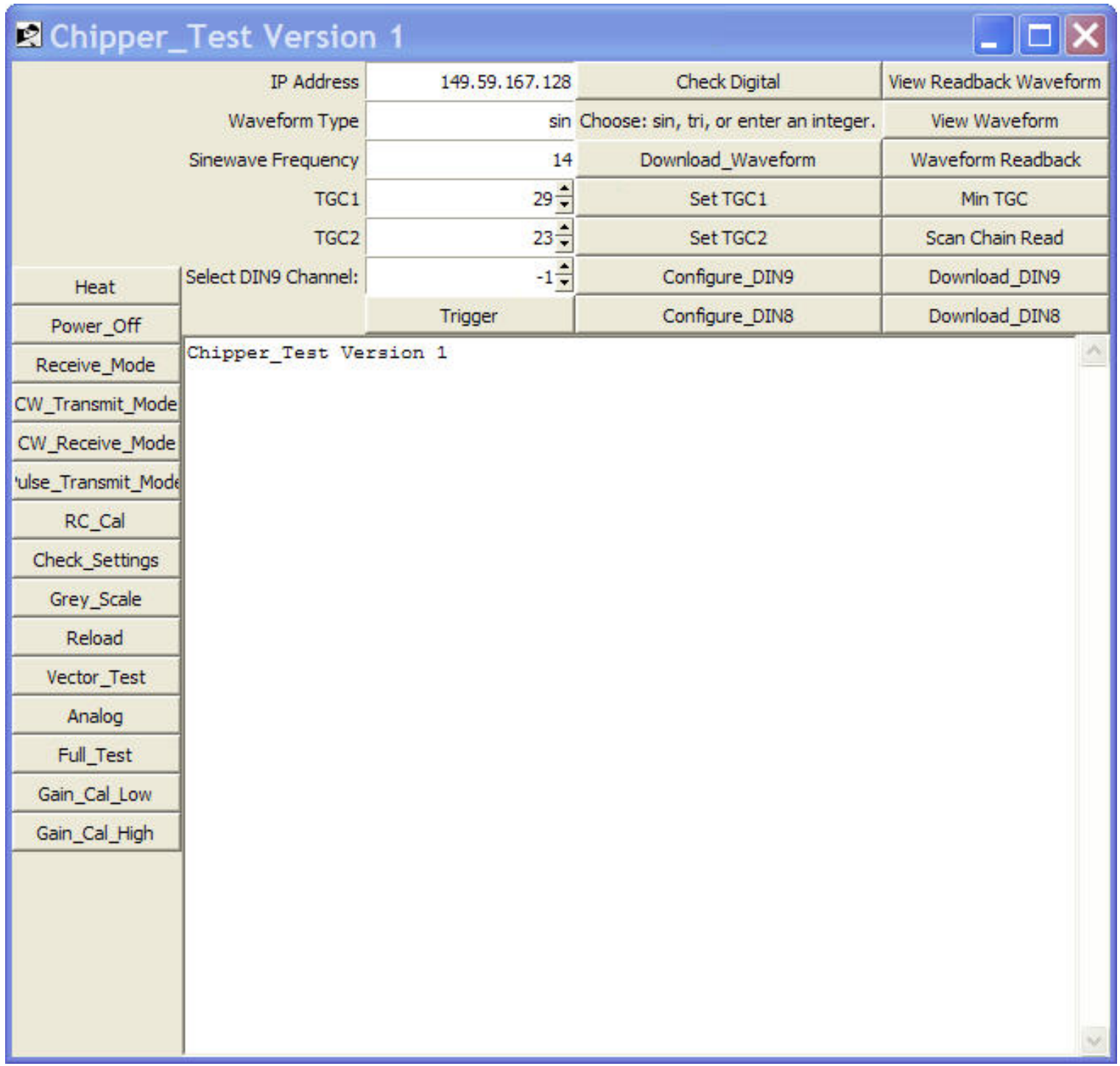
Step THREE - Create CPLD firmware:

```
CD7..CD0 pin 1,3,4,8,9,10,11,13 istype ‘reg,keep’;
CA5..CA0 pin 31,32,33,35,37,38 istype ‘reg,keep’;
        control_data = [CD7..CD0]  #we define the control_data set as 8 registers, one for each bit.
   control_addr = [CA5..CA0]  #we define the control_addr set as 6 registers, one for each bit.
        when (CDS & CW & control_addr== 8) then wf_data:= control_data;
   else wf_data:=wf_data;
```

Scan Chain Download Diagram



Chipper Software GUI



Key Points

Data transfer rate from computer to test stand: 675ns/byte

Example: The Chipper per line data stream is 56 bytes so total transfer takes: 37.8us

Complete vector test time: ~20 seconds, 800 vectors

Software is platform independent

Generic test stand uses a static IP address. Users can remotely operate board.

The TCL software commands specific to the test stand are highly documented.

Time to finish ASIC specific pcb layout: ~1-2wks (Chipper specific: 1wk)

Cost: 5 pcbs from Advanced Circuits on a 5 day turn: $66/board

Features Coming Soon

1. Design scripts to convert from TCL test vectors to WGL format for use at OnSemi.
2. Design scripts to convert WGL format back to TCL test vectors.