16-Ch/Dual 8-Ch High-Performance CMOS Analog Multiplexers

FEATURES

- Low On-Resistance—$r_{DS(on)}$: 50 Ω
- Low Charge Injection—Q: 15 pC
- Fast Transition Time—$t_{TRANS:}$ 200 ns
- Low Power: 0.2 mW
- Single Supply Capability
- 44-V Supply Max Rating

BENEFITS

- Higher Accuracy
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness
- Wide Supply Ranges: ±5 V to ±20 V

APPLICATIONS

- Data Acquisition Systems
- Audio Signal Routing
- Medical Instrumentation
- ATE Systems
- Battery Powered Systems
- High-Rel Systems
- Single Supply Systems

DESCRIPTION

The DG406 is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407 selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406/407 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications. For additional application information order Faxback document numbers 70601 and 70604.

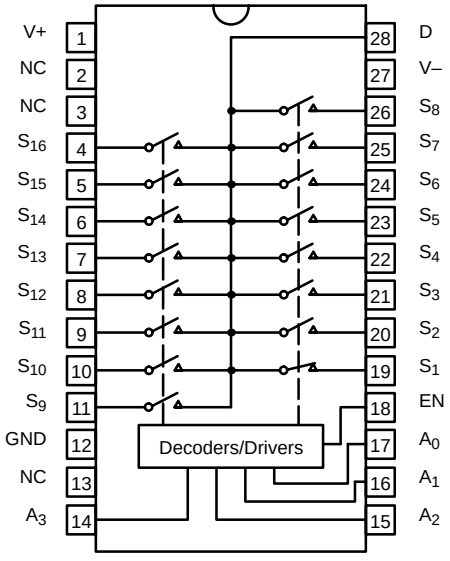
Designed in the 44-V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts, allowing operation with ±20-V supplies. Additionally single (12-V) supply operation is allowed. An epitaxial layer prevents latchup.

For applications information please request FaxBack documents 70601 and 70604.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406

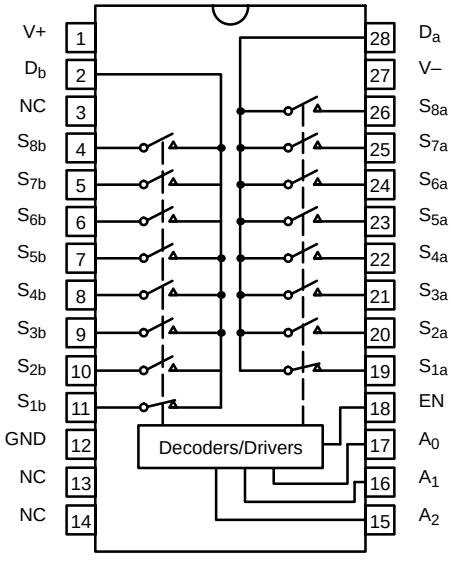
Dual-In-Line and SOIC Wide-Body



Top View

DG407

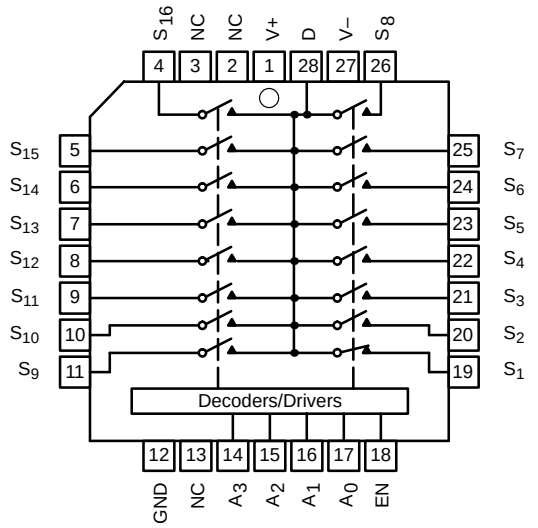
Dual-In-Line and SOIC Wide-Body



Top View

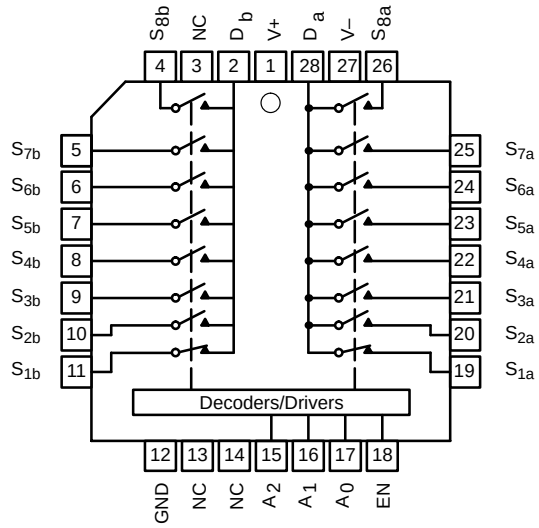
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406 PLCC and LCC



Top View

DG407 PLCC and LCC



Top View

TRUTH TABLE — DG406

A_3	A_2	A_1	A_0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

TRUTH TABLE — DG407

A_2	A_1	A_0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic “0” = $V_{AL} \leq 0.8$ V
Logic “1” = $V_{AH} \geq 2.4$ V
X = Don’t Care

ORDERING INFORMATION — DG406

Temp Range	Package	Part Number
–40 to 85°C	28-Pin Plastic DIP	DG406DJ
	28-Pin PLCC	DG406DN
	28-Pin Widebody SOIC	DG406DW
–55 to 125°C	28-Pin CerDIP	DG406AK/883, 5962-9562301QXA
	LCC-28	DG406AZ/883, 5962-9562301Q3A

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–55 to 125°C	28-Pin CerDIP	DG407AK/883’ 5962-9562302QXA
	LCC-28	DG407AZ/883 5962-9562302Q3A

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ . . . . . 44 V

GND . . . . . 25 V

Digital Inputs[a], V_S, V_D . . . . . (V–) –2 V to (V+) +2 V or 20 mA, whichever occurs first

Current (Any Terminal,) . . . . . 30 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) . . . . . 100 mA

Storage Temperature (AK, AZ Suffix) . . . . . –65 to 150°C
(DJ, DN Suffix) . . . . . –65 to 125°C

Power Dissipation (Package)[b]

28-Pin Plastic DIP[c] . . . . . 625 mW

28-Pin CerDIP[d] . . . . . 1.2 W

28-Pin Plastic PLCC[c] . . . . . 450 mW

LCC-28[e] . . . . . 1.35 W

28-Pin Widebody SOIC . . . . . 450 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 75°C
e. Derate 13.5 mW/°C above 75°C

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V, V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = –10 mA Sequence Each Switch On		Room Full	50		100 125		100 125	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$	V_D = ±10 V		Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V V_D = ±10 V V_S = ∓10 V		Room Full	0.01	–0.5 –50	0.5 50	–0.5 –5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$		DG406	Room Full	0.04	–1 –200	1 200	–1 –40	1 40	
			DG407	Room Full	0.04	–1 –100	1 100	–1 –20	1 20	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V Sequence Each Switch On	DG406	Room Full	0.04	–1 –200	1 200	–1 –40	1 40	
			DG407	Room Full	0.04	–1 –100	1 100	–1 –20	1 20	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{AH}	V_A = 2.4 V, 15 V		Full		–1	1	–1	1	µA
Logic Low Input Current	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		–1	1	–1	1	
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	7					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Room Full	200		350 450		350 450	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room Full	50	25 10		25 10		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room Full	150		200 400		200 400	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room Full	70		150 300		150 300	
Charge Injection	Q	C_L = 1 nF, V_S = 0 V, R_s = 0 Ω		Room	15					pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ f = 100 kHz		Room	–69					dB
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz		Room	8					pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 1 MHz		Room	130					
			DG407	Room	65					
Drain On Capacitance	$C_{D(on)}$		DG406	Room	140					
			DG407	Room	70					

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V_{EN} = V_A = 0 or 5 V	Room Full	13		30 75		30 75	µA
Negative Supply Current	I–		Room Full	–0.01	–1 –10		–1 –10		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V	Room Full	50		500 900		500 700	
Negative Supply Current	I–		Room Full	–0.01	–20 –20		–20 –20		

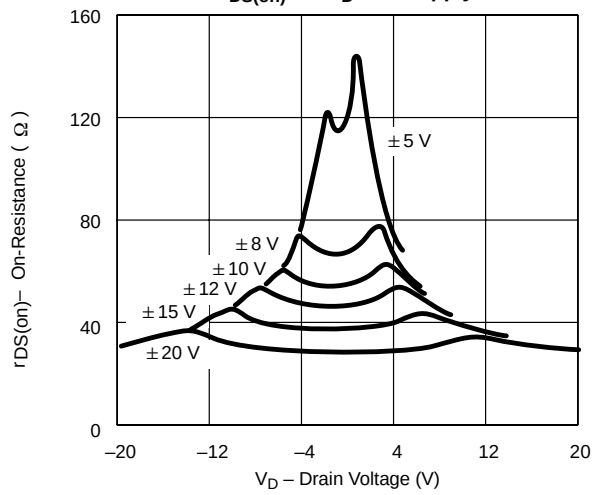
SPECIFICATIONS[a] FOR SINGLE SUPPLY

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V– = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, 10 V, I_S = – 1 mA Sequence Each Switch On		Room	90		120		120	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$			Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V V_D = 10 V or 0.5 V V_S = 0.5 V or 10 V		Room	0.01					nA
Drain Off Leakage Current	$I_{D(off)}$		DG406	Room	0.04					
			DG407	Room	0.04					
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V Sequence Each Switch On	DG406	Room	0.04					
			DG407	Room	0.04					
Dynamic Characteristics										
Switching Time of Multiplexer	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V		Room	300		450		450	ns
Enable Turn-On Time	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V V_{S1} = 5 V		Room	250		600		600	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	150		300		300	
Charge Injection	Q	C_L = 1 nF, V_S= 6 V, R_S = 0		Room	20					pC
Power Supplies										
Positive Supply Current	I+	V_{EN} = 0 V or 5 V, V_A = 0 V or 5 V		Room Full	13		30 75		30 75	µA
Negative Supply Current	I–			Room Full	–0.01	–20 –20		–20 –20		

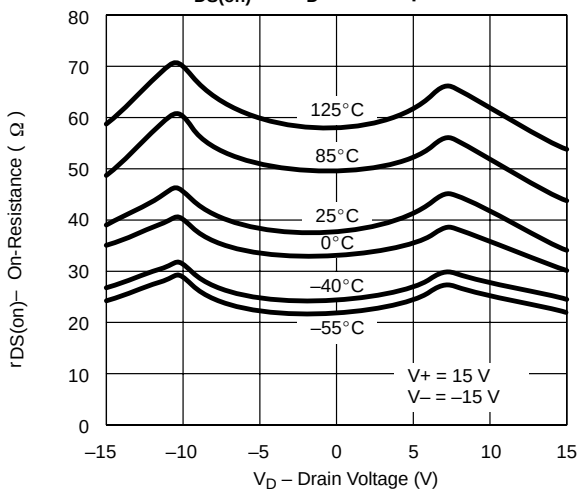
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)} = r_{DS(on)}$ MAX – $r_{DS(on)}$ MIN.
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

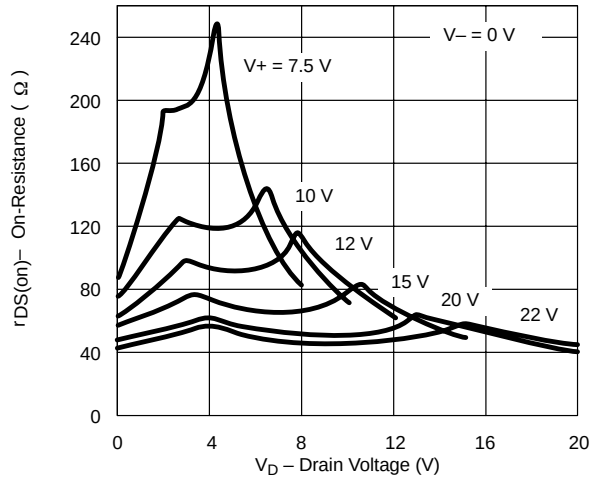
$r_{DS(on)}$ vs. V_D and Supply



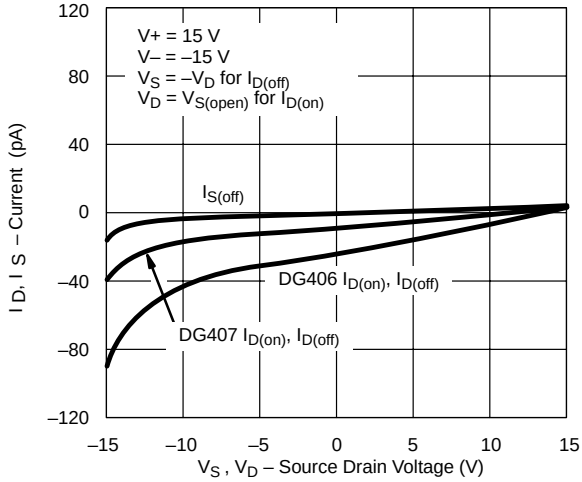
$r_{DS(on)}$ vs. V_D and Temperature



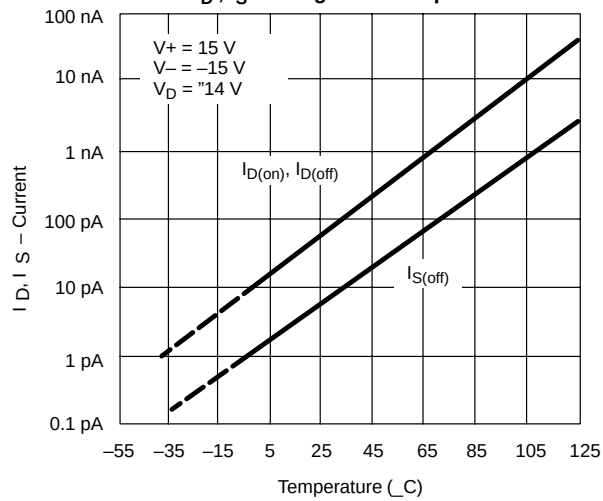
$r_{DS(on)}$ vs. V_D and Supply



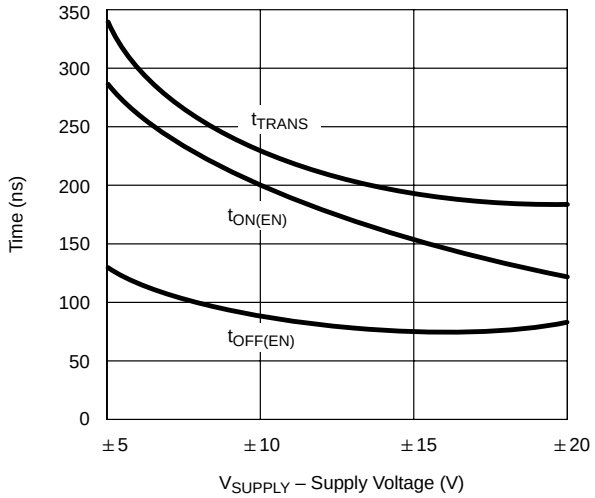
I_D , I_S Leakage Currents vs. Analog Voltage



I_D , I_S Leakages vs. Temperature

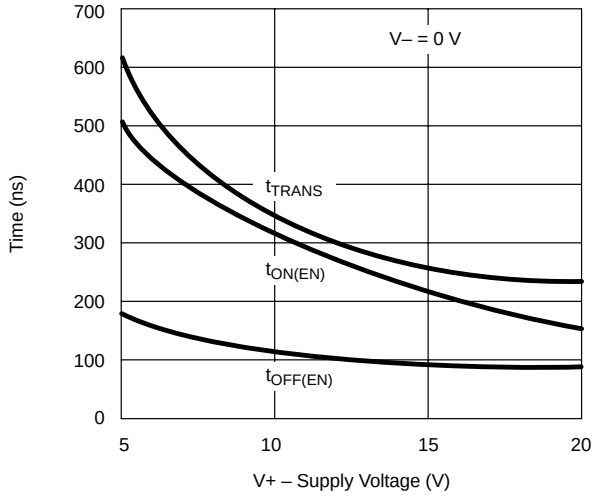


Switching Times vs. Bipolar Supplies

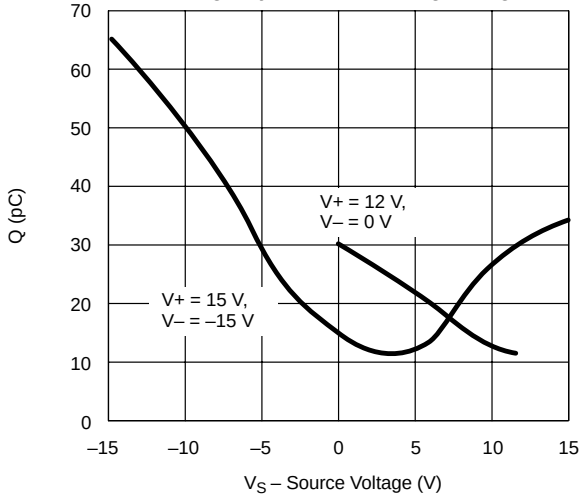


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

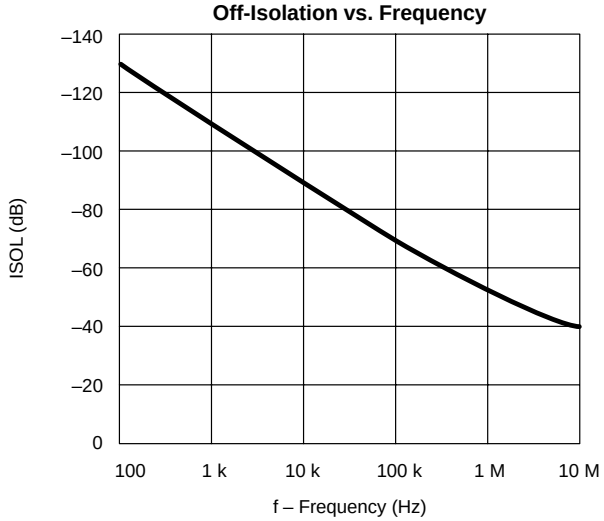
Switching Times vs. Single Supply



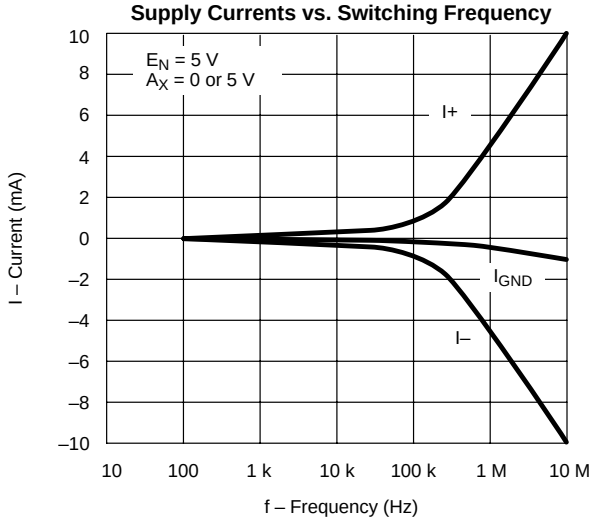
Charge Injection vs. Analog Voltage



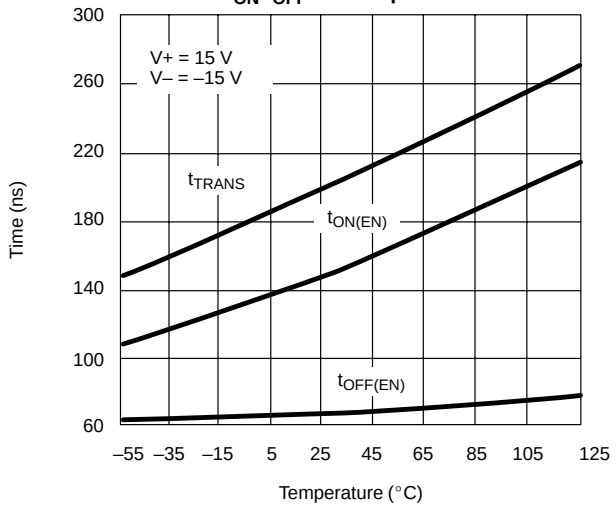
Off-Isolation vs. Frequency



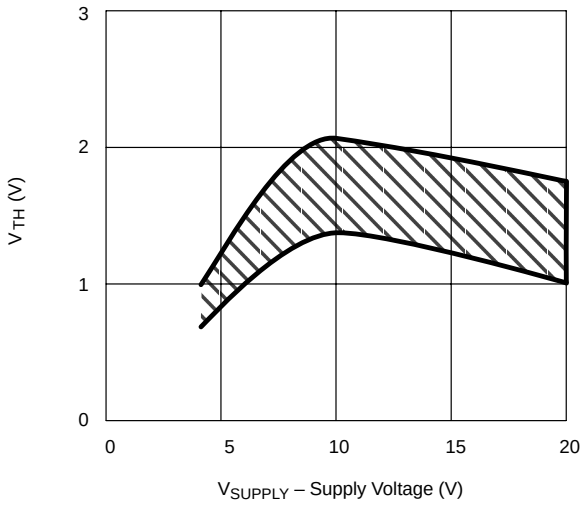
Supply Currents vs. Switching Frequency



t_{ON}/t_{OFF} vs. Temperature



Switching Threshold vs. Supply Voltage



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SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

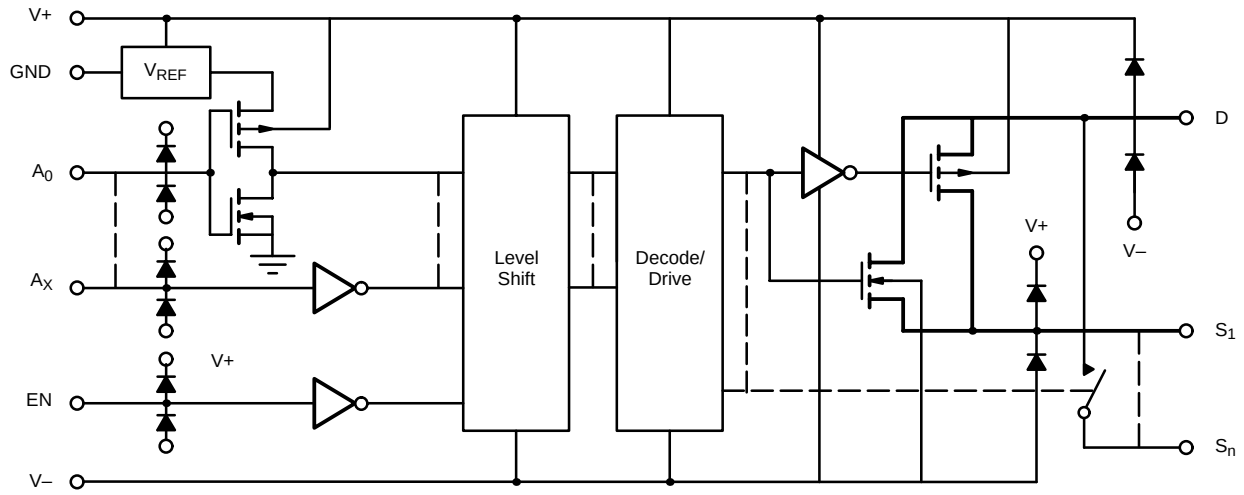
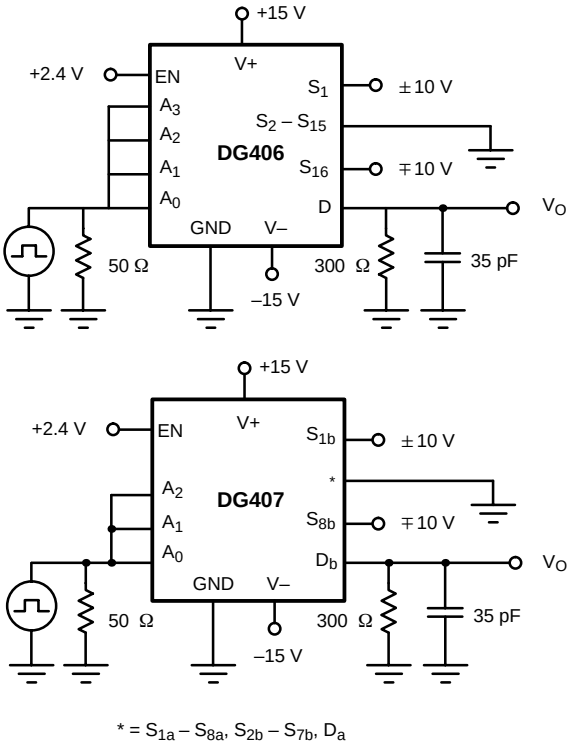


FIGURE 1.

TEST CIRCUITS



* = S_{1a} – S_{8a}, S_{2b} – S_{7b}, D_a

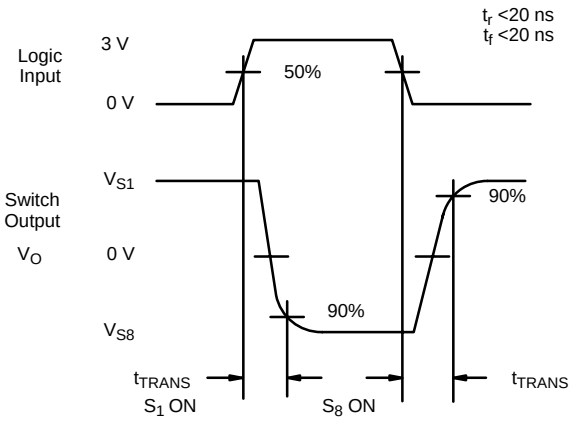


FIGURE 2. Transition Time

TEST CIRCUITS

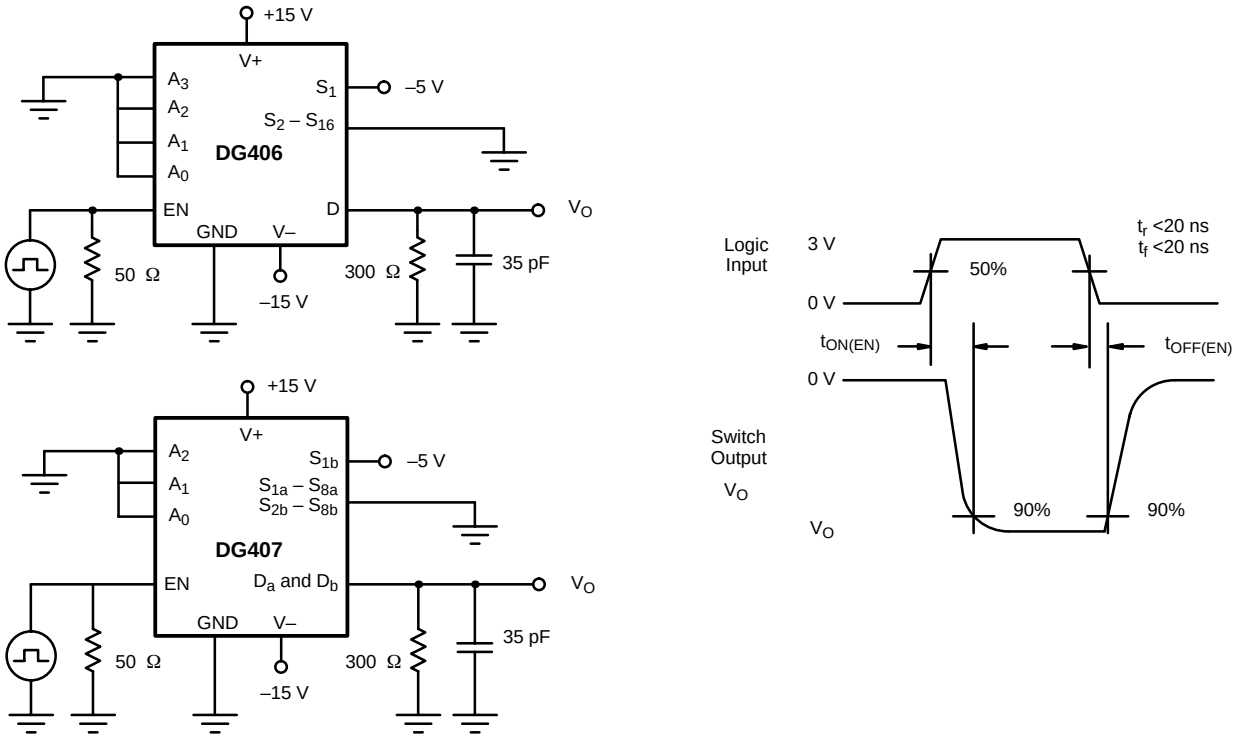


FIGURE 3. Enable Switching Time

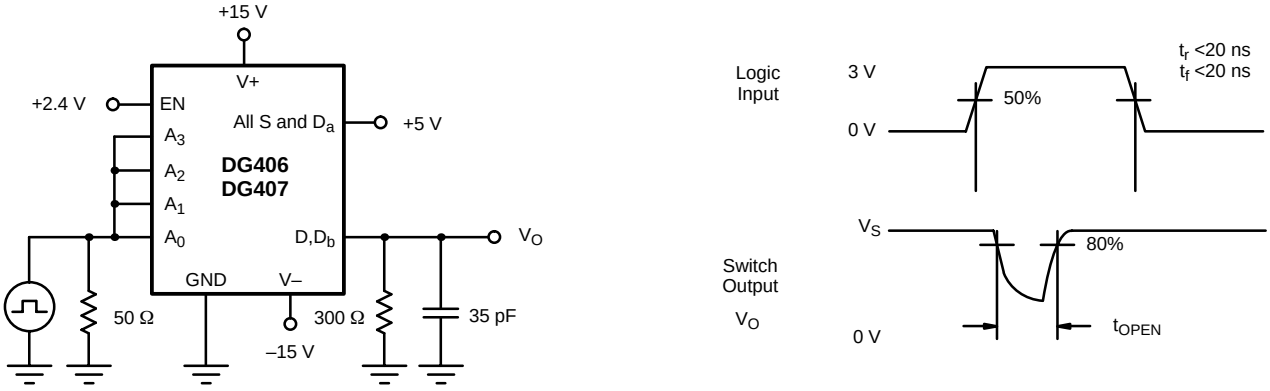


FIGURE 4. Break-Before-Make Interval

APPLICATION HINTS

Sampling speed is limited by two consecutive events: the transition time of the multiplexer, and the settling time of the sampled signal at the output.

t_{TRANS} is given on the data sheet. Settling time at the load depends on several parameters: $r_{DS(on)}$ of the multiplexer, source impedance, multiplexer and load capacitances, charge injection of the multiplexer and accuracy desired.

The settling time for the multiplexer alone can be derived from the model shown in Figure 5. Assuming a low impedance signal source like that presented by an op amp or a buffer amplifier, the settling time of the RC network for a given accuracy is equal to $n\tau$:

% ACCURACY	# BITS	N
0.25	8	6
0.012	12	9
0.0017	15	11

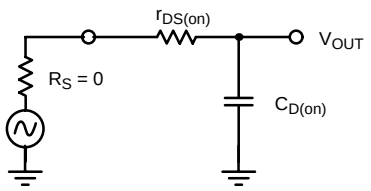


FIGURE 5. Simplified Model of One Multiplexer Channel

The maximum sampling frequency of the multiplexer is:

$$f_s = \frac{1}{N\,(t_{SETTLING} + t_{TRANS})} \qquad (1)$$

where N = number of channels to scan
$t_{SETTLING} = n\tau = n \times r_{DS(on)} \times C_{D(on)}$

For the DG406 then, at room temp and for 12-bit accuracy, using the maximum limits:

$$f_s = \frac{1}{16\,(9 \times 100\ \Omega \times 10^{-12}\text{F}) + 300 \times 10^{-12}\ \text{s}} \qquad (2)$$

or

$$f_s = 694\ \text{kHz} \qquad (3)$$

From the sampling theorem, to properly recover the original signal, the sampling frequency should be more than twice the maximum component frequency of the original signal. This assumes perfect bandlimiting. In a real application sampling at three to four times the filter cutoff frequency is a good practice.

Therefore from equation 2 above:

$$f_c = \frac{1}{4} \times f_s = 173\ \text{kHz} \qquad (4)$$

From this we can see that the DG406 can be used to sample 16 different signals whose maximum component frequency can be as high as 173 kHz. If for example, two channels are used to double sample the same incoming signal then its cutoff frequency can be doubled.

The block diagram shown in Figure 6 illustrates a typical data acquisition front end suitable for low-level analog signals. Differential multiplexing of small signals is preferred since this method helps to reject any common mode noise. This is especially important when the sensors are located at a distance and it may eliminate the need for individual amplifiers. A low $r_{DS(on)}$, low leakage multiplexer like the DG407 helps to reduce measurement errors. The low power dissipation of the DG407 minimizes on-chip thermal gradients which can cause errors due to temperature mismatch along the parasitic thermocouple paths. Please refer to Application Note AN203 for additional information.

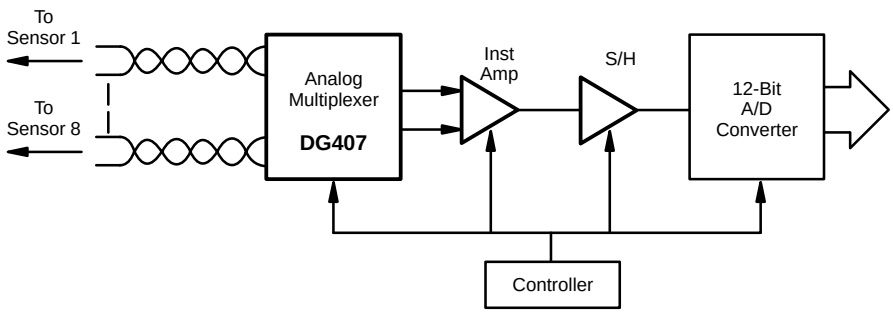


FIGURE 6. Measuring low-level analog signals is more accurate when using a differential multiplexing technique.